WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode; and

a frame rate conversion portion, wherein:

a display signal is input to the plurality of pixel electrodes through the plurality of switching elements;

all of the display signals input to the plurality of pixel electrodes have the same polarity within each frame period, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

2. A semiconductor device comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode; a plurality of source signal lines; and

a frame rate conversion portion, wherein:

a display signal input to the plurality of source signal lines is then input to the plurality of pixel electrodes through the plurality of switching elements;

within each frame period: display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines which are adjacent to the plurality of source signal lines; and the display signals input to each of the plurality of source signal line always have the same polarity, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

3. A semiconductor device comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

a display signal input to the plurality of source signal lines is then input to the plurality of pixel electrodes through the plurality of switching elements;

within each frame period: the display signals input to all of the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

4. A semiconductor device comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode; a plurality of source signal lines; and

a frame rate conversion portion, wherein:

a display signal input to the plurality of source signal lines is input to the plurality of pixel electrodes through the plurality

of switching elements;

within each frame period: display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

5. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; and

a frame rate conversion portion, wherein:

each of the plurality of pixels has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are then input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

6. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both converted into analog signals in a D/A converter circuit, and then input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

7. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements;

within each frame period, all of the display signals input to the pixel electrodes have the same polarity, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is

read out a second time.

8. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both converted into analog signals in a D/A converter circuit, and then input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements;

within each frame period, all of the display signals input to

the pixel electrodes have the same polarity, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

9. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the plurality of source signal lines and through the switching elements;

within each frame period: display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines; and the display signals input to the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

10. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; a plurality of source signal lines; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel

electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both converted into analog signals in a D/A converter circuit and then input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the plurality of source signal lines and through the switching elements;

within each frame period: display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines; and the display signals input to the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM

or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

11. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the plurality of source signal lines and through the switching elements;

within each line period, the display signals input to all of the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

12. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both converted into analog signals in a D/A converter circuit, and then input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements;

within each line period, the display signals input to all of the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is

read out a second time.

13. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit; a plurality of source signal lines; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements;

display signals having mutually inverse polarities, with the

electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines within each frame period;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

14. A semiconductor display device comprising:

a pixel portion having a plurality of pixels;

a source signal line driver circuit;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

the plurality of pixels each has: a switching element; a pixel electrode; and an opposing electrode;

the frame rate conversion portion has one RAM, or a plurality of RAMs;

image signals are written into the one RAM, or into one of the plurality of RAMs;

the image signals written into the one RAM, or into one of the plurality of RAMs, are each read out twice;

the image signals which are read out twice from the one RAM or from one of the plurality of RAMs are both converted into analog signals in a D/A converter circuit, and then input to the source signal line driver circuit;

two display signals are generated by the source signal line driver circuit;

the two display signals have mutually inverted polarities;

the two generated display signals are input to the pixel electrodes through the switching elements;

display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines within each frame period;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference; and

a period in which one image signal is written into the one RAM or is written into one of the plurality of RAMs is longer than a period during which the written in image signal is read out a first time, and longer than a period during which the written in image signal is read out a second time.

15. A semiconductor display device according to any one of claims 5 to 14, wherein the RAM is an SRAM, a DRAM, or an SDRAM.

16. A semiconductor display device according to any one of claims 1 to 15, wherein the switching element is: a transistor formed using single crystal silicon; a thin film transistor formed using polycrystalline silicon; or a thin film transistor formed using amorphous silicon.

17. A computer using the semiconductor display device according to any one of claims 1 to 16.

18. A video camera using the semiconductor display device according to any one of claims 1 to 16.

19. A DVD player using the semiconductor display device according to any one of claims 1 to 16.

20. A method of driving a semiconductor display device, comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode; and

a frame rate conversion portion, wherein:

display signals are input to the plurality of pixel electrodes through the plurality of switching elements;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

21. A method of driving a semiconductor display device, comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode; and

a frame rate conversion portion, wherein:

display signals are input to the plurality of pixel electrodes through the plurality of switching elements;

all display signals input to the plurality of pixel electrodes have the same polarity within each frame period, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

22. A method of driving a semiconductor display device, comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

display signals input to the plurality of source signal lines are then input to the plurality of pixel electrodes through the plurality of switching elements;

within each frame period: display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines; and the display signals input to the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

23. A method of driving a semiconductor display device, comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

display signals input to the plurality of source signal lines are then input to the plurality of pixel electrodes through the plurality of switching elements;

within each line period, the display signals input to all of the plurality of source signal lines always have the same polarity, with the electric potential of the opposing electrode as a reference;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal

input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.

24. A method of driving a semiconductor display device, comprising:

a plurality of switching elements;

a plurality of pixel electrodes;

an opposing electrode;

a plurality of source signal lines; and

a frame rate conversion portion, wherein:

display signals input to the plurality of source signal lines are then input to the plurality of pixel electrodes through the plurality of switching elements;

display signals having mutually inverse polarities, with the electric potential of the opposing electrode as a reference, are input to source signal lines adjacent to the plurality of source signal lines within each frame period;

the polarities of the display signals input to the plurality of source signal lines are mutually inverted in adjacent line periods, with the electric potential of the opposing electrode as a reference;

the frame rate conversion portion operates in synchronous with the display signals; and

among two arbitrary, adjacent frame periods, the display signal input to the plurality of pixels in the latter frame period to appear has an electric potential which is an inversion of the display signal input to the plurality of pixels in the former frame period, with the electric potential of the opposing electrode as a reference.